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Description

A METHOD FOR PRINTING MARKS ON THE EDGES OF WAFERS

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention generally relates to repeated pattern exposure on semiconductor wafers, and more particularly to a process that erases alignment marks as it steps across the wafer so that alignment marks only remain on the edge of the wafer.

[0003] Description of the Related Art

[0004] Semiconductor device fabrication is achieved by lithographical exposures of multiple layers of repeating arrays of circuitry patterns on a wafer. The circuitry patterns of the chips on a wafer are surrounded by non-active regions (kerf regions) that have scribe features used for alignment marks, overlay marks, electrical structures, and other process monitoring structures. In addition to the repeating chip images, scribe features also repeat across the wafer. However, not all scribe features are useful for every single exposure. Inclusion of such non-active features increases the overall die dimension and decreases the number of dies per wafer, which increases unit cost.

SUMMARY OF INVENTION

[0005] The present invention details a method of printing marks or features on edges of a repeating array of images, using a mask or reticle in a semiconductor manufacturing (lithography) process. The invention addresses the utility of printing these edge marks on a very limited number of areas, thereby saving valuable space. The invention also provides a methodology of printing features in areas where alignment marks were previously printed. The information printed in these areas can include critical dimension (CD); electrical; film thickness; and other process characterization features.

[0006] More specifically, the invention provides a method of repeatedly exposing a pattern across a wafer in a sequential stepping process. The pattern that is exposed includes at least one alignment mark. Each time the exposing process is repeated, the current exposure overlaps a portion of the wafer where the pattern was previously exposed and thereby erases a previously exposed alignment mark by re-exposing an area of the wafer where the previously exposed alignment mark was located. After the exposing process is repeated across the wafer, alignment marks remain only on the edge of the wafer.

[0007] In other words, the invention repeatedly exposes a pattern across a wafer by exposing the pattern at a first location (e.g., first semiconductor chip) of the wafer and repeating the exposing process across the wafer, such that the pattern is repeatedly printed across the wafer. Again, this process erases the alignment mark from portions of the wafer where the pattern was previously exposed. The mask

includes a transparent region at a location where an image produced by a subsequent exposing process overlaps a previously exposed alignment mark so that the previous alignment mark is erased. The areas of exposure overlap comprise kerf regions (e.g., support regions of the wafer positioned between semiconductor chips). The sequential stepping process can be either a light-field exposure process or a dark-field exposure process.

[0008] The invention produces a wafer that has a plurality of semiconductor chips (or similarly printed areas) where the alignment marks are positioned only along one edge of the wafer. In such a structure, each of the semiconductor chips is identical across the wafer. The alignment marks are in a first location with respect to remaining features of respective semiconductor chips located along the edge of the wafer. The other semiconductor chips, that are not along the edge of the wafer, include other exposed patterns (that are not alignment marks) in their respective first locations.

BRIEF DESCRIPTION OF DRAWINGS

[0009] The invention will be better understood from the following detailed description of preferred embodiments with reference to the drawings, in which:

[0010] Figure 1 is a schematic diagram of a portion of a mask;

[0011] Figure 2 is a schematic diagram of a portion of a mask;

[0012] Figure3 is schematic diagram of a portion of a mask according to the

invention;

[0013] Figure4 is schematic diagram of a portion of a mask according to the invention;

[0014] Figure 5 is a schematic diagram of an array of exposure patterns on a semiconductor chip with conventional alignment markings;

[0015] Figure 6 is a schematic diagram of an array of exposure patterns on a semiconductor chip with the inventive alignment markings;

[0016] Figure 7 is a schematic diagram of an array of exposure patterns on a semiconductor chip with conventional alignment markings;

[0017] Figure 8 is a schematic diagram of an array of exposure patterns on a semiconductor chip with the inventive alignment markings;

[0018] Figure 9 is schematic diagram of a portion of a mask according to the invention;

[0019] Figure 10 is a schematic diagram of an array of exposure patterns on a semiconductor chip with the inventive alignment markings; and

[0020] Figure 11 is a schematic diagram of the wafer illustrating the alignment marks appearing only along one edge of the wafer.

DETAILED DESCRIPTION

[0021]

Currently, alignment marks are printed across all image fields on a wafer. Figures 1 and 2 show one mask or reticle. Alternatively, Figures 1-2 (and Figures 3-4) can show the pattern that will be printed with such

masks. Further, in this disclosure the term mask and reticle are used interchangeably and are considered the same or equivalent structures. The invention is equally useful with masks that contain multiple alignment marks. Also, the central portion of the drawings would normally include many mask details that form the structures of the integrated circuit chip. Such internal structures have been intentionally omitted from the drawings so as to focus the viewer's attention on the alignment marks and the salient features of the invention. Such a mask or reticle could be either regular chrome on glass without phase shifting, un-shifted attenuated or alternating phase shift in design. Essentially, each of the squares in Figures 1-4 represents a single integrated circuit chip that would be printed on a wafer. As shown in Figures 5-8, 10, and 11, multiple integrated circuit chips are formed on the wafer. The integrated circuit chips are separated by kerf regions 201, shown in Figure 11, which are areas that will be cut away and discarded when the wafer is diced into individual chips.

[0022]

In Figure 1, the scribe mark feature 10 and protect shape 11 are opaque regions (chrome) that are blocked from exposure during the lithographic process. Figure 1 shows the protect-shape 11 for a light-field reticle that is used to prevent printing over or on top of previously printed scribe marks 10 when the images are stepped across a wafer according to a defined periodicity. Figure 2 shows the reversed polarity of a light-field reticle (e.g., a dark-field). In Figure 2, the scribe mark feature is exposed and no protect-shape is required. Either one of the

reticle types (light-field or dark-field) can be used for chip fabrication.

[0023] Figures 3 and 4 illustrate the inventive method using a light-field reticle (also known as a correct positive design) and a dark-field reticle (also known as a correct negative design) respectively. In Figure 3, the scribe mark 10, labeled F, is also printed but without a protect-shape 11, which is intentionally removed as shown by item 30. With the protect-shape 11 removed, the scribe mark 10 is erased (re-exposed or overexposed) when the neighboring image is exposed during the lithographic process. Similarly, in Figure 4, a dark-field reticle will have a clear-out shape so that, when the image is stepped, the scribe mark feature is printed over or erased.

[0024] Figures 5 and 6 show exposed arrays of images 50 using the light-field masks shown in Figures 1 and 3, respectively. Each image 50 represents a single integrated circuit chip. Figure 5 shows that the scribe mark feature 10 is printed for every image on the wafer because of the protect-shape on the reticle in Figure 1. However, Figure 6 is formed according to the mask shown in Figure 3 and shows that the scribe mark features are restricted to the edge of the array; that is, the outermost images. This is accomplished by the neighboring image stepping one periodicity away, labeled I-1, and printing over (erasing) the exposed scribe feature 10 of the previously exposed field, labeled I-2.

[0025] For a dark-field reticle, Figures 7 and 8 show the difference between the masks shown in Figures 2 and 4, respectively. In Figure 7, all scribe

marks 10 are printed for each image (chip) 50. On the other hand, Figure 8 shows that the scribe marks 10 are only printed on the outermost edge of the array. This is because the clear-out image 40 exposes the area of the wafer where the scribe marks 10 are printed over so as to erase the scribe marks 10. Figures 6 and 8 both show how the current invention can create space in the interior of the array. This space can be used at subsequent steps for printing other useful features.

[0026]

Thus, the invention provides a method of repeatedly exposing a pattern across a wafer in a sequential stepping process. The pattern that is exposed includes at least one alignment mark 10. Each time the exposing process is repeated, the current exposure overlaps a portion of the wafer where the pattern was previously exposed. As shown in Figures 1-4, the mask is wider than the field stepping periodicy, which allows each subsequent exposure to overlap a portion of a previous exposure during the stepping process. In the figures, the masks are designed to be stepped from right to left across the wafer. Therefore, the protect shape 11 will overlap the previously exposed alignment mark 10 in the next subsequent exposure step. Similarly, the clear out shape 40 will overlap a previously exposed scribe mark feature 10 in the next subsequent exposure step. The invention erases (re-exposes, overexposes) a previously exposed alignment mark by re-exposing an area of the wafer where the previously exposed alignment mark was located. After the exposing process is repeated across the wafer,

alignment marks remain only in the last exposed areas of the wafer.

[0027] Thus, the invention repeatedly exposes a pattern (e.g., Figures 3-4) across a wafer by exposing the pattern at a first location (e.g., first semiconductor chip I2) of the wafer and repeating the exposing process across the wafer (e.g., at I1), such that the pattern is repeatedly printed across the wafer (in this example from right to left across the wafer). Again, this process erases the alignment mark 10 from portions of the wafer where the pattern was previously exposed (I2). The mask includes a transparent region (e.g., clear out shape 40 or absence of a protect shape 30) at a location where an image produced by a subsequent exposing process overlaps a previously exposed alignment mark so that the previous alignment mark is erased. The areas of exposure overlap comprise kerf regions (e.g., support regions of the wafer positioned between semiconductor chips).

[0028] Figures 9 and 10 illustrate how the invention utilizes the space saved by limiting the alignment marks to one edge of the wafer. More specifically, Figures 9 and 10 illustrates a reticle 90 having a second different scribe mark feature 91, labeled F2. This reticle 90 would be used in a subsequent stepping process. This scribe mark feature 91 is not necessarily another alignment mark. To the contrary, the scribe mark 91 could comprise critical dimension (CD); electrical; film thickness; and other process characterization features. When this reticle 90 is stepped over the array, shown in Figure 10, the subsequent scribe mark feature 91 is printed in the available space without printing

over the first feature 10. In order to avoid it printing over the alignment mark 10, the reticle 90 can include a protect shape 92 or other similar feature. The dark-field mask is constructed the same way and the same result appears. Thus, the forgoing demonstrates that two different features (10 and 90) can be place in the same periodic spacing without any extra lithography steps.

[0029] Figure 11 illustrates many advantages produced by the invention. More specifically, Figure 11 illustrates a wafer 200 that includes the inventive alignment marks 10 positioned only along the left-hand edge exposures. In addition, Figure 11 illustrates the secondary mark 91 printed within the kerf 201 regions. As shown by item 60, the marks are only printed along the left-hand edge of the wafer 200 without being printed in areas where they are not needed. Item 61 shows that a non-yielding exposure field 50 can be shifted (by an amount required) to not overlap with the neighboring field. Specific shifting is programmed into the exposure recipe file. Item 62 shows that an exposure 202 can be omitted from the stepping sequence if this exposure is not-yielding (will not produce a good semiconductor chip) and if the printing of the alignment mark 10 will not occur within the central region of the wafer 200. Item 63 illustrates that a non-yielding edge ship can be bladed or framed so as to accommodate printing of the alignment marks 10 on where exposure 50 would otherwise have been printed.

[0030] Items 61, 62 and 63 are methods to achieve the desired result of this invention (of printing edge marks). There are three conventional ways

of printing edge marks. One way is to drop marks from another reticle. The disadvantage of this is that it requires the use of two reticles, with reticle swap occurring for each wafer to be exposed. This also requires re-adjusting the framing blades in the tool for each reticle swap. Another conventional way is to open the framing blade to expose a mark in the outer kerf area. This requires enough room on the reticle but it is, otherwise, similar to item 63 in terms of time required. The third conventional way is to drop marks from the same reticle. This requires framing all four sides of the reticle and more programming of the recipe file to specify the mark exposure position.

[0031] Thus, as shown above, the invention prints alignment marks only on edge which frees up scribe space for other useful purposes. This procedure saves more time than if one was to drop-in marks at the edge and, is simpler in design. If one were to drop-in marks only along the edge locations, this would require four framing blade movements and a different stepping within the step-and-scan or a step-and-repeat exposure system. To the contrary, the methodology discussed above only one blade movement and no stepping change, or no blade movements and one stepping change. This invention utilizes a mask design that, in one shot, exposes alignment marks specifically at the edge while also erasing un-wanted or un-needed marks in the inner region of the wafer. The simplicity of the inventive design can reduce the errors associated when programming marks are to be dropped.

[0032] While the invention has been described in terms of preferred

embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.